



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/811,461	03/26/2004	Marius K. Orlowski	SC13240TP	1781
23125	7590	09/29/2005	EXAMINER	
FREESCALE SEMICONDUCTOR, INC. LAW DEPARTMENT 7700 WEST PARMER LANE MD:TX32/PL02 AUSTIN, TX 78729			BOOTH, RICHARD A	
			ART UNIT	PAPER NUMBER
			2812	

DATE MAILED: 09/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/811,461	ORLOWSKI ET AL.	
	Examiner	Art Unit	
	Richard A. Booth	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on _____.
- 2a) This action is **FINAL**. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-29 is/are pending in the application.
 - 4a) Of the above claim(s) 1-15 is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 16-29 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
 Paper No(s)/Mail Date 0304.
- 4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date. _____.
- 5) Notice of Informal Patent Application (PTO-152)
- 6) Other: _____.

DETAILED ACTION

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

- I. Claims 1-15, drawn to a semiconductor device, classified in class 257, subclass 413.
- II. Claims 16-29, drawn to a method of making a semiconductor device, classified in class 438, subclass 592.

The inventions are distinct, each from the other because of the following reasons:

Inventions II and I are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case, the product as claimed can be made by another and materially different process, for instance, instead of selectively removing portions of the first and second patterned conductive layers, these layers could be selectively formed in the notched configuration.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

During a telephone conversation with Kim Marie Vo a provisional election was made with traverse to prosecute the invention of group II, claims 16-29. Affirmation of this election must be made by applicant in replying to this Office action. Claims 1-15

Art Unit: 2812

are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 16-17, 19, and 23-29 are rejected under 35 U.S.C. 102(e) as being anticipated by Mansoori et al., US 2005/0014353.

Mansoori et al. shows the invention as claimed including a method for forming a semiconductor device comprising: providing a substrate 1602 having a surface; forming an insulating layer 1604 over the surface of the substrate; forming a first patterned conductive layer 1620 over the insulating layer; forming a second patterned conductive layer 1610 over the first patterned conductive layer; forming a patterned non-insulating

layer 1614 over the second patterned conductive layer; and selectively removing portions of the first and second patterned conductive layers to form a notched control electrode for the semiconductor device (see figs. 15-25 and paragraphs 0036-0061).

With respect to claim 17, note that the process further comprises implanting source/drain regions 1636/1638 in the substrate (see fig. 24).

Regarding claim 19, note that the patterned non-insulating layer is polysilicon.

Concerning claims 23-24, note that the second patterned conductive layer is silicon-germanium.

Regarding claim 25, Mansoori et al. teaches the use of aluminum oxide as a gate dielectric.

With respect to claims 26-27, note the process steps of: selectively etching a predetermined portion of an exposed lateral edge of the second patterned conductive layer; and oxidizing an exposed portion of the first patterned conductive layer to form a layer 1630,1632.

Regarding claims 28-29, note that the process further comprises forming a second insulating sidewall layer 1630,1632 in the notches and on the opposite sides of the notched control electrode.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mansoori et al., US 2005/0014353.

Mansoori et al. is applied as above but does not expressly disclose wherein the first patterned conductive layer is formed to a thickness of between 1 and 40 nanometers. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to determine through routine experimentation the optimum thickness of the first conductive layer based upon a variety of factors including the particular desired scaling of the semiconductor device and such limitation would not lend patentability to the instant application absent a showing of unexpected results.

Claims 18 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mansoori et al., US 2005/0014353 in view of Pidin et al., "A Notched Metal Gate MOSFET for sub-0.1 micron Operation".

Mansoori et al. is applied as above but does not expressly disclose forming a halo implant in the substrate or forming the first patterned conductive layer of a material such as titanium nitride.

Pidin et al. discloses a notched gate whereby a high concentration halo channel implant is performed in the substrate (see fig. 1) and the first conductive layer is formed of titanium nitride (see fig. 8). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Mansoori et al. so as to perform a halo implant and form the first conductive layer of titanium nitride because such an implant forms a MOSFET device with good electrical characteristics, and because a material such as titanium nitride is an excellent conductor to be used in gate formation.

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mansoori et al., US 2005/0014353 in view of Gardner et al., U.S. Patent 6,225,168.

Mansoori et al. is applied as above but does not expressly disclose forming the first conductive layer of a material such as tungsten.

Gardner et al. discloses forming a gate with a first conductive material 209 which can be formed of tantalum nitride (see col. 3-lines 10-24). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Mansoori et al. so as to form the first conductive layer of tantalum nitride because this layer provides a good barrier for the gate electrode from the gate dielectric.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard A. Booth whose telephone number is (571) 272-1668. The examiner can normally be reached on Monday-Thursday from 7:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Richard A. Booth
Primary Examiner
Art Unit 2812

September 28, 2005